Overview on Some Recent Advances in Wafer Bonding Technologies

H. Moriceau[1], F. Fournel[1,2], O. Rayssac[1,3], A. Soubie[1], B. Bataillou[1], B. Aspar[1], K. Rousseau[2], N. Magnéa[2], C. Maleville[3], T. Barge[3]
[1]-CEA/LETI – Département de Technologie Silicium
[2]-CEA/DRFMC – SiNaPS
17, Rue des Martyrs, F38054 Grenoble Cedex 9 - France
[3]-SOITEC, Parc technologique des Fontaines, Bernin
38926 Crolles Cedex - France

Recent advances in hydrophilic or hydrophobic direct bonding technologies have led to both developments of silicon on insulator (SOI) structures and emergence of new applications. Hereafter, we present recent results on various homo- or hetero-structures realised by molecular adhesion. Physical parameters and surface chemical bonds, mainly involved in bonding mechanisms, are highlighted by characterisation before contacting the two wafers and after bonding. Effects due to additional thermal treatments are also emphasised.

In microelectronics, one of the most convincing examples of hydrophilic molecular adhesions remains the bonding of Si-OH terminated silicon surfaces, as used in SOI bonded structures. Beyond the crystalline quality, a way for SOI structure developments deals with achievement of thinner or thicker structures. For micro-electronic applications, ultra thin SOI wafers, made of Si and SiO_2 layers a hundred nanometers thick and below, were successfully transferred by the Smart-cut® process, in which a wafer bonding step is included. For example, (~.1µm Si/~.1µm SiO_2) SOI structures were produced. High crystalline qualities and thickness uniformities were achieved, comparable to those of standard (.2µm Si/.4µm SiO_2) SOI structures, over the whole 200mm wafer. Further actions to reduce thickness in the 0.05µm regime with the same level of quality are underway.

At the opposite, for high power device applications for which thicker buried SiO_2 layers (up to ~3 µm) and (10 to 60 µm) thick silicon layers are needed, classical BSOI techniques were used in parallel with the Smart-cut® process. Thermal treatments were tuned to achieve thick SOI structures with low bows and warping.

Beyond these quasi-standard SOI wafers, multi-layered structures are more and more emergent. (Si-SiO_2) bilayers were periodically bonded, up to 4 [Si(110 nm)/SiO_2(260 nm)] periods [1]. Role of both surface micro-roughness and surface cleaning before bonding was highlighted, evidencing that SOI surfaces, as-achieved by the Smart cut® process, were suitable to direct bonding.

More recently, .2µm thick silicon film on insulating multi-layered (SOIM) were successfully carried out by the Smart-cut® process [2]. For instance, insulating multi-layers were achieved by bonding SiO_2 films to Si_3N_4 films, the thickness of each one being in the range [~0 to .4µm]. Because of its high thermal dissipation power, Si_3N_4 film is specially attractive, as buried insulating layer, in devices submitted to self heating effect. In this multi-layering process, main bonding parameters were tuned, such as a low surface micro-roughness or a quite hydrophilic behaviour. Effects of layer thickness ratios and thermal treatment temperatures were evaluated, leading to control either positive or negative bows. Bonding mechanism was investigated by FTIR-MIT [3], evidencing Si-$(O$-$N)_x$-Si bonds when treatment temperatures had been over 900°C.

Similarly, Si-Si hydrophobic bonding has lead to new emerging technologies. Surfaces are HF last treated before contacting. First studies based on bonding of two Si bulk wafers were previously published [4]. For few years [5], new substrates for self-organised deposition of nano-structures (such as few nm wide quantum dots) have been investigated, by bonding thin 100mm Si films to 100mm Si wafers. Buried at the crystalline bonding interface, the screw and edge dislocation networks induce periodic strain fields at the surface of these substrates. As a matter of fact, in plane rotations of crystalline axes (twist) lead to screw dislocations and surface inclinations (tilt), mainly due to silicon wafer dicing, induce mixed dislocations. Providing to control the twist and the tilt angles during the direct bonding, lattice parameter of a self organised nano-structure network can be selected. So, 2.75° twisted and ~0.34° tilted bonded structure was achieved, with a 10 nm thick top silicon layer. TEM observations highlighted respectively square networks, linked to the screw dislocations, with a 8 nm lattice parameter, and a linear periodic grid, due to mixed ones, with a 46 nm period (figure 1).

More generally, using the Smart-cut® process to transfer thin films, hetero-structures were successfully achieved with SiC, AsGa, (S-, Sn-, or Zn-) doped InP, insulating InP, Ge, $LiNbO_3$…films, enlarging the field of applications in micro-electronics, opto-electronics, micro-waves, and sensors. Usually, most of the film transfers are tuned first by wafer bonding onto silicon wafers and then onto substrates suitable to their applications (fused silica, poly-crystalline SiC, sapphire, Si via a metallic film…)

To conclude, wafer direct bonding processes, already in production for SOI structures, appear also as very promising technologies well adapted to many material combinations. Furthermore, it can be especially emphasized that the generic Smart-cut® process allows to achieve many new hetero-structures.

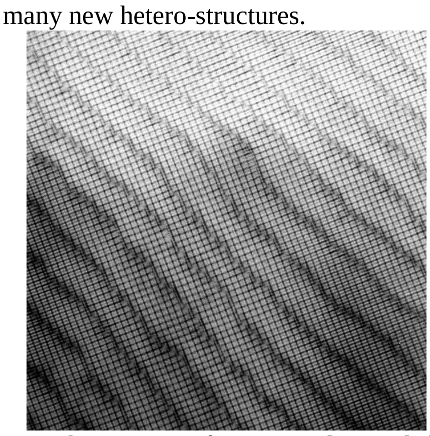

Fig.1: TEM observation of screw and mixed dislocation networks in Si/Si bonded structure (2.75° twist, .34° tilt).

[1] C. Maleville, T. Barge, B. Ghyselen, A.J. Auberton, H. Moriceau, A.M. Cartier, 2000 IEEE Intern. SOI Conference, p.134.
[2] O. Rayssac, H. Moriceau, M. Olivier, I. Stoemenos, A. M. Cartier, B. Aspar, *SOI Technology and Devices X*, PV **01-03**, 39, E.C.S. Proceedings, Pennington, NJ (2001)
[3] C. Maleville, O. Rayssac, H. Moriceau, B. Biasse, L. Baroux, B. Aspar, M. Bruel, *Semiconductor wafer bonding, Science Technology and Applications IV*, PV **97-36**, 46, E.C.S. Proceedings, Pennington, NJ (1998).
[4] M. Benamara, A. Rocher, L. Laanab, A. Claverie, A. Laporte, G. Sarrabayrousse, L. Lescouzeres, A. Peyre-Lavigne, Comptes-Rendus-de-l'Académie-des-Sciences,-Série-II, vol.318, no.11; 2 June 1994; p.1459-64
[5] F. Fournel, H. Moriceau, N. Magnea, J. Eymery, J.L. Rouviere, K. Rousseau, B. Aspar, Mat. Science Eng. B, vol.B73, no.1-3; 3 April 2000, p.42-6.